



Modelling for Multiport Converter-Based Hybrid Power Supply using Renewable Energy Source Applications

Yalisho Girma^{1*}, Dr. Ing. Getachew Biru², CS. Reddy¹

¹Adama Science & Technology University (ASTU), Ethiopia

²Addis Ababa Institute of Technology (AAiT), AAU, Ethiopia

*Corresponding Author's Email: yalishogirma1983@gmail.com

Abstract

This study focuses on the design and modeling of a multiport converter-based hybrid power supply that uses solar PV to meet the needs of a small village. The village has a maximum power demand of 50 kW, serving twenty households. The first converter in the proposed multiport system is a high-frequency isolated DC-DC converter powered by an HVDC link, producing an output of 240 VDC. This converter employs a medium-frequency transformer with converters on both the primary and secondary sides, arranged in an input-series output-parallel (ISOP) configuration. Its output is connected to a solar PV and battery system through a buck-boost converter. The second converter is a three-phase modular inverter powered by the solar PV system, designed to supply an AC line voltage of 0.415 kV. The inverter is driven by a solar PV module with an open-circuit voltage of 85 V and a maximum power output of 415 W. To evaluate the system's performance, scenarios involving changes in load and solar irradiance were analyzed. Performance was measured using indicators such as output voltage THD, current distortion, variations in converter output voltage, current magnitude, and overall efficiency. The system was modeled and simulated using the Simulink/PLECS (Piecewise Linear Electrical Circuit Simulation) platform. The simulation results indicate that the proposed multiport converter system serves as a promising alternative to the traditional low-frequency distribution transformer.

Keywords: DC-DC Converter, Hybrid Power Supply, MMC, Multiport Converter, Solar PV, Distribution Transformer

I. Introduction

The high carbon emission due to the use of fossil fuel-fired power plants, coupled with high environmental concerns in recent times pushed the conventional electric distribution system to integrate more and more renewable energy sources (RES) and modern energy distribution infrastructures. Integrating renewable energy sources (RES) into conventional electrical distribution systems requires the active involvement of power electronic converters. Traditional centralized distribution systems depend on low-frequency

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



transformers, which are unable to meet the additional demands of modern networks. Today's distribution systems require bidirectional power and data flow, seamless integration of distributed energy resources and energy storage, load compensation, and improved power quality and reliability.

A multiport power electronic converter-based power supply system can be viewed as an alternative option to a low-frequency transformer to supply both DC and AC loads. In the multiport converter-based power supply system, both DC port and AC port are available, with the function of using distributed energy resources (Solar PV, battery energy system, micro-wind, etc.), AC loads, and DC loads. An isolated DC-DC converter contains a pulse-width modulated inverter at the primary side, a high-frequency transformer, and a PWM secondary rectifier. The input to the isolated DC-DC converter can be an HVDC or modular rectifier connected to the AC grid. The presence of HFT greatly reduces the size and volume of the system to be designed. The modular multilevel inverter is another key element in the multiport converter-based power supply. This component takes a DC input voltage at the output of the DC-DC stage or solar PV and converts it into AC.

Since disturbances in the low-voltage (LV) grid often occur due to the frequent switching on and off of heavy loads, an output grid filter—both common-mode and differential-mode—is required. Using readily available power switches with low blocking voltages (1.2 kV, 1.7 kV, and 3.3 kV) is a well-established and widely adopted industrial practice for developing power processing converters at this stage. However, this stage also faces challenges related to high current. To manage the high current demand, interleaved PWM and input-series output-parallel (ISOP) converter topologies can be employed.

The presence of a neutral conductor is another essential requirement at this stage, as low-voltage distribution networks typically follow a Terra-Terra (TT) configuration. Additionally, load imbalance and non-linearity—both of which generate zero-sequence currents—must be effectively addressed in three-phase three-wire or three-phase four-wire systems. The most suitable inverter topologies for this application include the conventional two-level voltage source inverter (VSI), the three-level neutral point clamped (NPC) inverter, and the T-type inverter [1].

However, two-level and three-level converters are associated with high conduction losses, switching losses (both turn-on and turn-off), and significant dV/dt stress due to the need for high-frequency operation. To develop highly efficient and reliable inverters, modular inverter configurations such as Cascaded H-Bridge (CHB) or Modular Multilevel Converter (MMC) topologies with low switching frequency operation can be utilized.



CHB- and MMC-based modular converters offer several advantages, including modularity at both the cell and phase levels, simple voltage and power scalability through the combination of identical cells, and the use of a single capacitor for energy storage in each module. They also enable faulty cells to be easily bypassed during faults, providing fault ride-through capability. Additional benefits include low dV/dt , reduced electromagnetic interference (EMI), cost-effectiveness, good transient response, and the use of commonly available low-voltage power switches. However, these advantages come at the expense of requiring a larger number of passive and active components compared to non-modular systems [2]–[4].

The CHB-based modular inverter requires separate cell voltage, and this may cause complexity in system size and control design. A modular inverter based on MMC topology doesn't need a separate module DC voltage and hence is the focus of this research. A literature survey shows that different PWM techniques have been discussed to operate a modular inverter [2]–[4]. Sub-module capacitor voltage unbalancing is a common problem in MMC and studies conducted [6] have justified the causes of capacitor voltage balancing problems and the strategy to reduce the problem. The input source to the MMC MMC-based modular inverter can be a solar PV battery bank in this research as the location of the project site (Arba Minch) has good solar energy potential as compared with other RES such as wind. The design and modeling of a multiport converter-based hybrid power supply for the small village (Ayssa Residence) in Arba Minch City is the focus of this study.

The remaining sections of this paper are organized as follows: Section Two presents a description of the study area and the layout diagram of the proposed system. Section three includes research methodology, a review of the converter configurations, the basic working principles, a mathematical approach to analyzing MMC, multicarrier PWM techniques, solar PV sizing, and the design of a buck-boost DC-DC converter. Simulation results and a discussion of the proposed system for different scenarios are covered in Section 4. The last section of the paper is the conclusion.

II. Description of Study Area Site

The design research is done for Aysa's common residents, located in Arba Minch city and depicted in Fig. 1. The residence is located 7km from the main distribution substation and contains twenty (20) households having a connected load demand of 10kW per household, giving a total of 200kW. Each household has a maximum demand of 4kW and a system maximum demand of 50kW is obtained by considering a diversity factor of 1.6.

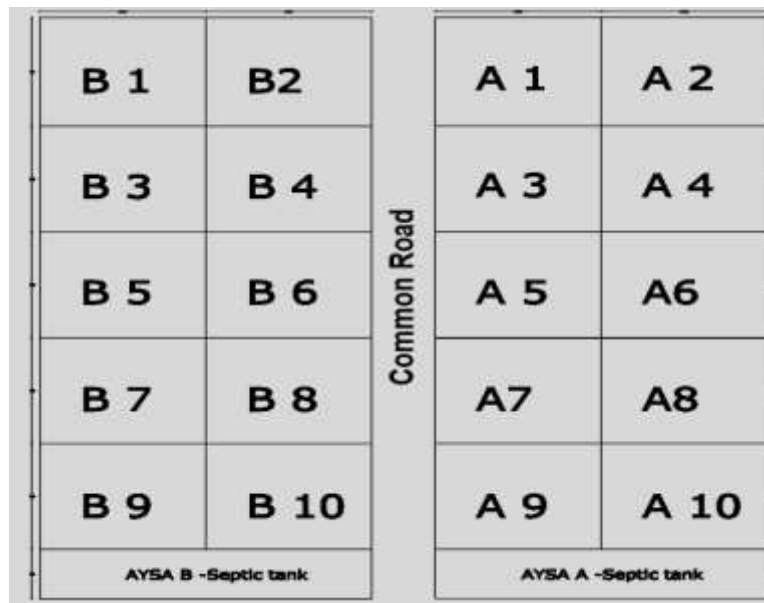


Fig. 1.: Description of Study Area (codes represent household buildings)

The proposed DC-AC hybrid power supply based on a multiport converter for the village is shown in Fig. 2.

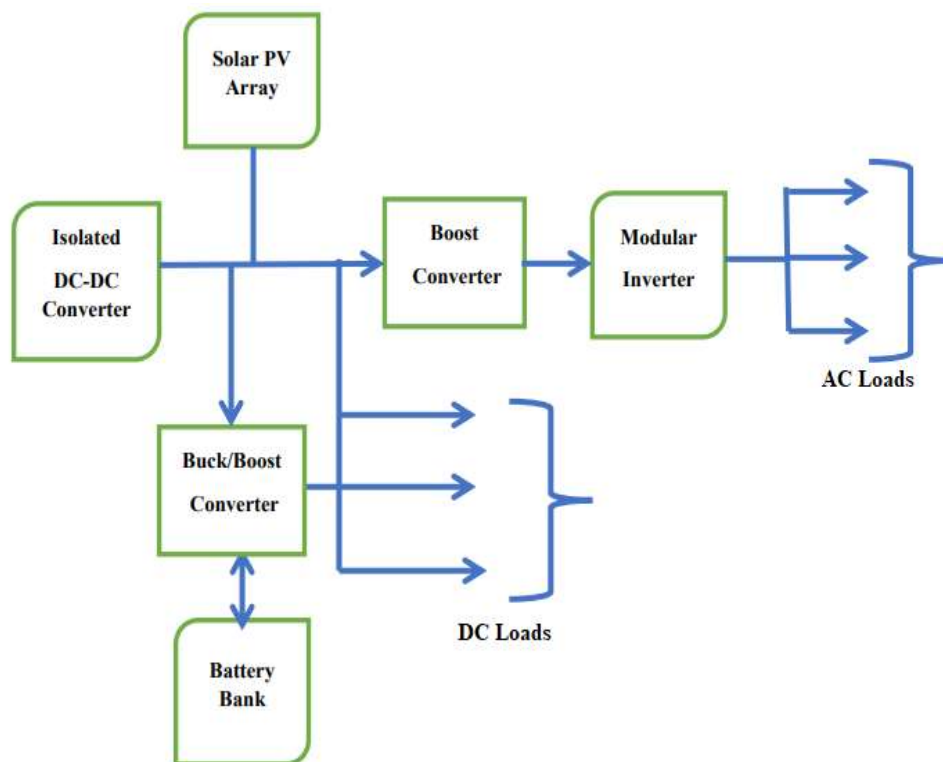


Fig. 2.: Layout of Proposed Multiport Converter-Based Hybrid Power Supply System

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



III. Research Methodology

This research used modeling and simulation to assess the performance of different converters. The power and modulation circuits of the system were modeled using the Simulink/PLECS simulation package, and their performance was tested under various conditions, including changes in load demand and solar irradiance. Key performance indicators, including output voltage distortion, current THD, and efficiency (losses), were analyzed. The study focuses on supplying a 50 kW load but can be scaled up for higher loads by adjusting the number of submodules per phase, as well as the number of PV modules and batteries.

A. Configuration of Isolated DC-DC Converter

The primary converter in the DC-DC stage receives 24.5 kV from the HVDC transmission network. Several converter topologies, such as standard DAB and MAB in both symmetrical and asymmetrical configurations, can be used. A three-phase DAB can also be applied at this stage, which helps reduce the size of the low-voltage capacitor. In this study, a symmetrical DAB in an ISOP configuration (Fig. 2) is selected for the DC-DC stage, and its performance is evaluated for comparison. The low-voltage DC output from this stage, which is supplied to the modular inverter, is 750 V. The efficiency of this stage depends on factors such as the type of transformer (three-phase or single-phase), its design, core material, and winding configuration. This stage operates at a high frequency, which helps reduce the size of passive components and space requirements. However, since high-voltage isolation limits the operating frequency, a maximum switching frequency of 20 kHz is recommended [19].

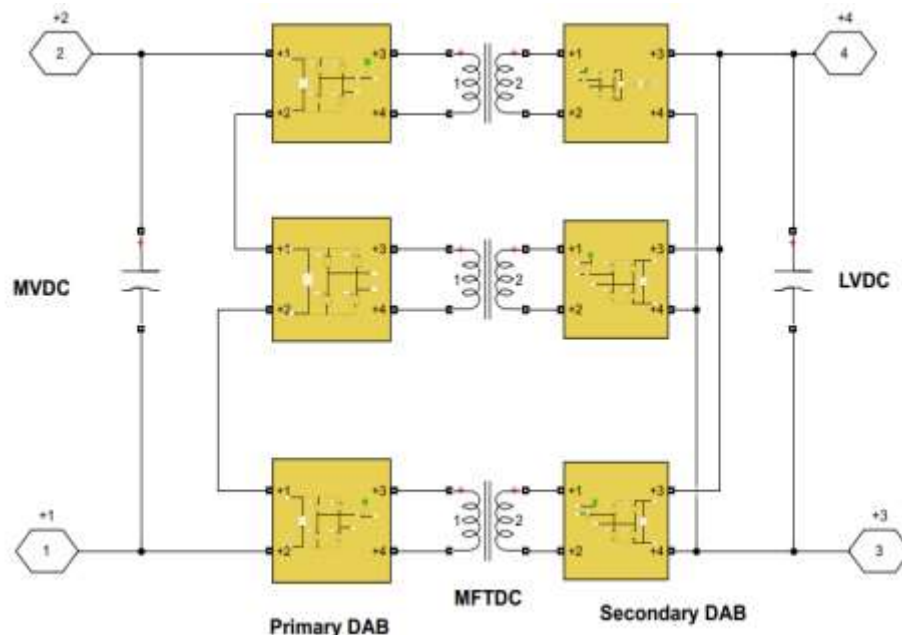


Fig. 2.: Isolated DC-DC Converter in ISOP Configuration

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



B. Primary and Secondary Side Converter Parameters for Proposed Topologies

As shown in the basic specification Table I of the DC-DC stage, the input to the PWM inverter or primary DAB is 24.5kV. For the DAB ISOP configuration shown in Fig. 2, the DC link voltage is shared equally in three primary DAB circuits. The peak rectangular AC voltage to each primary DAB should be slightly lower than the DC input to avoid over-modulation. Therefore, a value of $24.5\text{kV}/3 = 8.2\text{kV}$ is chosen as the peak AC rectangular voltage for each primary converter. The RMS value of primary DAB is calculated as:

$$V_{\text{RMS(P)}} = \frac{8.2\text{kV}}{\sqrt{2}} = 5.8\text{kV} \approx 6\text{kV} \quad (1)$$

Assuming that total power(S) is shared equally among the three primary DABs, the RMS primary currents for the three proposed configurations can be obtained as:

$$I_{\text{RMS(P)}} = \frac{S/3}{V_{\text{RMS(P)}}} = 2.77\text{A} \approx 3\text{A} \quad (2)$$

The LVDC requirement as given in the basic specification Table I, is 240V because at this stage, renewable energy resources such as PV can be interfaced. The MFT output (Secondary side) AC RMS voltage should be slightly less than the output LVDC voltage to avoid over-modulation. If we select a value of 230V, the MFT secondary peak voltage is $230\text{V} * \sqrt{2} = 325\text{V}$.

The MFT turns ratio is given by $\frac{V_P}{V_S} = 36:1$

In DAB_ISOP configurations, the value of the secondary side current is shared among the parallel-connected secondary DABs as a result of power sharing among the three secondary side converters

$$I_{\text{RMS(S)}} = \frac{S/3}{V_{\text{RMS(S)}}} = 72.5\text{A} \quad (3)$$

Based on the above analysis, the semiconductor switch ratings of the primary side and secondary side converters with sufficient consideration of safety factors are summarized in the Table I below.

Table I: Switching Device Parameter for DC-DC Stage

Primary side Voltage = 10Kv							
Device Company	PN and	I(A)	Ron (mΩ)	Eon/E-off (mJ)	VG(V)	Configuration	
CPM3-10000- 0270 (CREE)		20	300	6/1		DAB_ISOP,	
Secondary side Voltage = 900V							

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



Device	PN and Company	I(A)	Ron (mΩ)	Eon/Eoff(mJ)	Vf (V)	Configuration
SD11740 (Solitron)		100	8.6	3.5/0.7		DAB_ISOP

C. Configuration of Modular Inverter

Two-level and three-level VSIs face issues such as high dV/dt and di/dt , as well as limited intelligent operation for activating or deactivating modules during partial loading of the distribution grid. A suitable solution to these problems is to use multilevel inverters that operate with low-voltage switches and low switching frequencies, as discussed in [7]. Several topologies can serve as basic building blocks, but the half-bridge submodule shown in Fig. 3 is chosen because it requires fewer switches and therefore results in lower switching and conduction losses.

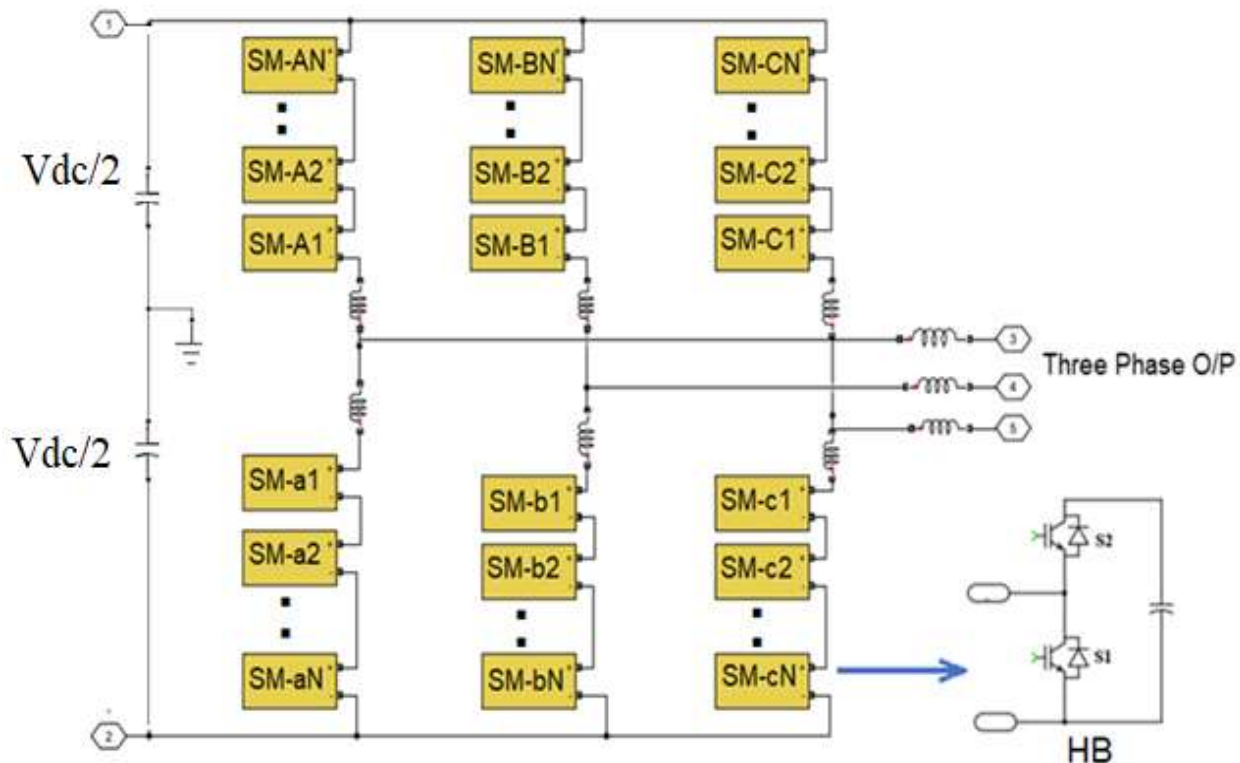


Fig. 3.: Modular Inverter

The half-bridge sub-module (HBSM) which is used as a basic building block can have four operation states based on the direction of current flow. When current flows into the capacitor or out of the capacitor, the sub-module is said to be in insertion mode, in which case current flows through the upper switch or upper diode. On the other hand, when current flows in the lower switch or lower diode, the sub-module is said to be in bypass mode, in which case the sub-module output voltage is zero.

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



1) Sizing of several sub-modules and passive components: - As shown in Fig.3, the MMC-based inverter is made of an N number of series connected sub-modules per phase leg. The phase legs contain arm inductance which limits the circulating current. The number of sub-modules per phase leg arm (N) is given by the equation below [8]: -

$$N \geq \frac{V_{DC}}{\eta V_{CES}} \quad (4)$$

Where, V_{CES} is the semiconductor blocking voltage η is the de-rating factor and V_{DC} is the DC link voltage.

If the DC link voltage at the inverter input terminal is 750V, a MOSFET with a blocking voltage of 200V and a device de-rating factor of 0.909 is used in the above equation, the number of sub-modules per phase leg arm becomes four (4).

Submodule capacitance (C_{SM}) as a function of apparent power, power factor, average capacitor voltage, acceptable ripple, switching frequency, and modulation index and number of sub-module is given as follows [8]: -

$$C_{SM} \geq \frac{S}{3NmV_C^2 \epsilon \omega} \left[1 - \left(\frac{m \cos \varphi}{2} \right)^2 \right]^{\frac{2}{3}} \quad (5)$$

The phase-leg arm inductance helps filter out circulating currents and limits the arm current during a fault. Based on the maximum ripples in the circulating current, the arm inductance can be given by the following expression as discussed in [8]: -

$$L_{arm} \geq 0.25 \frac{U_{C,MAX}}{N f_C \Delta i_{L,MAX}} \quad (6)$$

where $U_{C,MAX}$ is the maximum voltage of an SM capacitor; $\Delta i_{L,MAX}$ is the product of the maximum current ripple and the circulating current, N is the number of sub-modules and f_C is the switching frequency of each SM. It is a good practice to use the maximum current ripple of 15% as mentioned in [9].

The power electronic building block for the back-end converter is chosen based on the application type and the system's maximum-load current and voltage requirements. According to the power distribution specifications, the maximum load current is 70 A, and the line-to-line AC voltage is 415 V with a lagging power factor between 0.95 and 1. Therefore, MOSFETs with a blocking voltage of at least 200 V and a current rating of 130 A or higher are selected from manufacturers such as International Rectifier, Infineon, and others. A nine-level (9-level) back-end converter MMC topology is adopted for this project.

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



After reviewing the semiconductor device manufacturer's datasheet, the following power switch as depicted in Table II, was selected for simulation purposes:

Table II: Chosen Power Semiconductor Switches for the System

Device part number	Voltage rating (V)	Current rating(A) @25°C	Manufacturer
Power MOSFET (IRFP4668PbF)	200	130	IR

2) Converter power and semiconductor loss: - The input DC power to the converter and output AC power supplied by the converter can be related by:

$$P_{dc} = V_{dc}I_{dc} = P_{ac} + \text{losses} = 0.5m \frac{V_{dc}}{2} I_{pp} \cos \alpha + \text{Losses} \quad (7)$$

Power electronic system losses primarily originate from their components, including power devices and resistive elements (stray resistance). Due to the non-ideal nature of these components, three main types of losses occur: conduction losses, switching losses, and blocking losses. Among these, blocking losses—caused by minor leakage currents—are generally negligible and are often omitted in most analyses.

For power electronic devices that include a diode, such as MOSFETs with fast recovery diodes (FRD), losses must be calculated separately for the switch and the diode. Conduction losses occur when the MOSFET or FRD is on and carrying current. The conduction power loss is found by multiplying the on-state voltage by the on-state current. In applications using pulse-width modulation (PWM), this total conduction loss is further multiplied by the duty factor. The total conduction loss for a MOSFET with an integrated FRD can be expressed by the following equation.

$$P_{cond(tot)} = P_{cond(IGBT)} + P_{cond(Diode)} \quad (8)$$

$$P_{cond(MOSFET)} = \frac{1}{T} \int_0^T [V_{CE}(t) * I_C(t)] dt \quad (9)$$

The average conduction loss of IGBT can be computed by the following equation:

$$P_{av(cond)} = V_{CE(S)} * I_C * \delta \quad (10)$$

Where δ refers to the device duty cycle

The transitions of the MOSFET and FRD between on and off states do not happen instantly, which causes switching losses. During these transitions, both the current through the device and the voltage across it remain above zero, resulting in high instantaneous power losses.



Equations to determine the switching power losses for an IGBT and FRD are given below: -

$$P_{sw}(MOSFET) = E_{ON} + E_{OFF} * f_{SW} \quad (11)$$

$$P_{sw}(FRD) = E_{rec} * f_{SW} \quad (12)$$

The turn-on energy (E_{on}), turn-off energy (E_{off}) of the IGBT, and the reverse recovery energy (E_{rec}) of the FRD depend on factors such as collector current, collector voltage, gate resistance, and junction temperature.

It is important to normalize the switching losses for any application using the nominal values and conditions provided in the device datasheet.

$$P_{sw}(MOSFET) = \left(\frac{E_{ON} + E_{OFF}}{\pi} \right) * f_{SW} * \frac{I_{pk}}{I_{nom}} * \frac{V_{DC-link}}{V_{nom}} \quad (13)$$

$$P_{sw}(FRD) = (E_{rec}/\pi) * f_{SW} * I_{pk}/I_{nom} * V_{(DC-link)}/V_{nom} \quad (14)$$

By calculating the switching and conduction losses of the IGBT and FRD, the total loss can be determined, which helps in evaluating the system's efficiency and estimating the junction temperature of the devices.

$$P_{tot} = P_{Cond}(MOSFET) + P_{sw}(MOSFET) + P_{Cond}(FRD) + P_{sw}(FRD) \quad (15)$$

A piecewise linear electronics circuit system (PLECS) uses a lookup table, formula, or a combination of the lookup table and formula approach to determine conduction and switching losses [10]. The lookup approach estimates device loss values using interpolation and extrapolation methods based on data points from the datasheet. The novelty of this research lies in integrating device thermal models with converter efficiency calculation models. The thermal model for a single MOSFET with an integrated FRD is shown in Fig. 4. For power electronic systems with multiple switches, the same method can be applied using a common heat sink shared by all semiconductor switch packages. To calculate system efficiency, the periodic average of conduction losses and the periodic impulse average of switching losses obtained from probe outputs are combined, as illustrated in Fig. 5 [10].

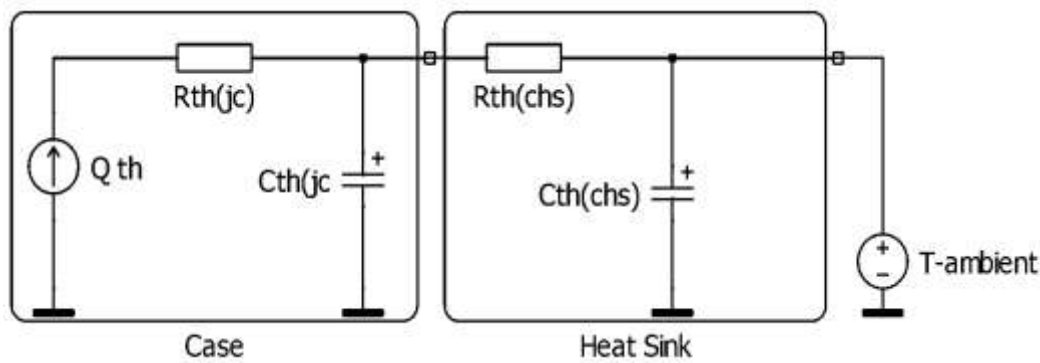


Fig. 4.: Thermal Model of a Single Semiconductor Device

Using the thermal data provided by the device manufacturer, switching and conduction losses are calculated through a combination of look-up tables and formula-based computations.

The converter efficiency calculation diagram shown in Fig. 5 uses thermal loss values to determine the system's efficiency. The efficiency analysis is performed using the thermal model of selected silicon carbide power MOSFETs. For the MMC converter, this is done by combining lookup tables and formulas for a maximum load current and a case temperature of 100°C . All thermal parameters are taken from the device manufacturers' datasheets [8], [11], [14]. Using the efficiency calculation model in Fig. 5, the switching loss, conduction loss, and total semiconductor loss of the converter for the selected submodules are calculated.

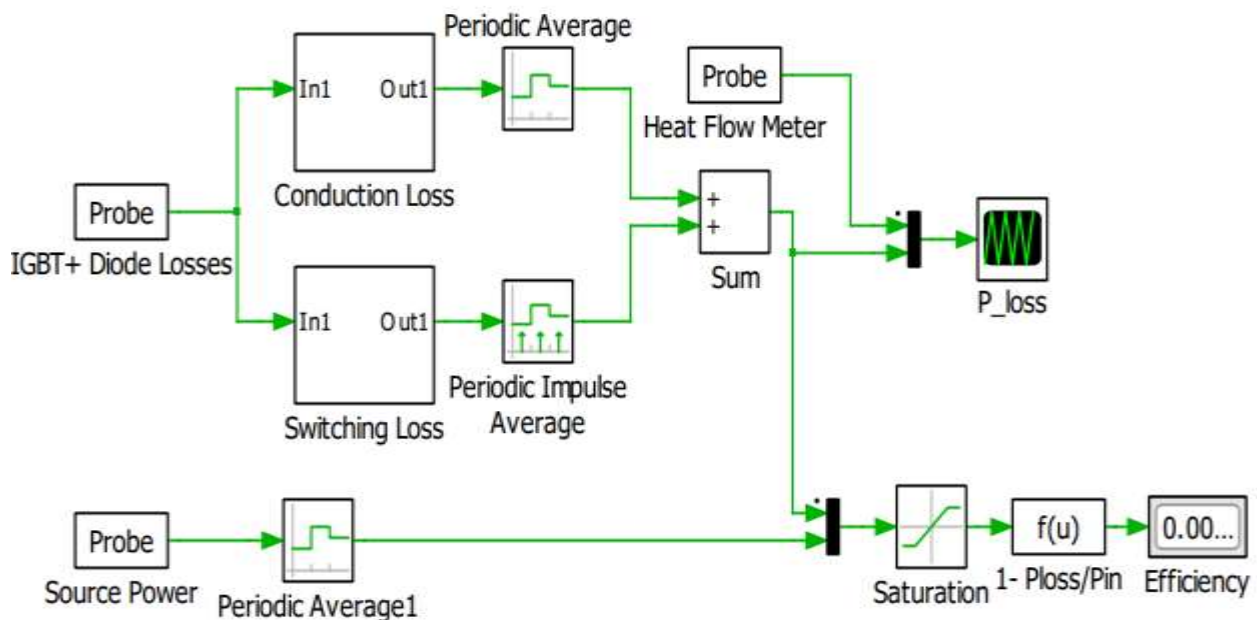


Fig. 5.: Efficiency Calculation Diagram

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



The efficiency of the converter system, as depicted in the model, is calculated as follows: -

$$\eta = \frac{P_{out}}{P_{in}} \quad (16)$$

Expressing P_{out} as a difference of P_{in} and power loss, the above expression is written as

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \quad (17)$$

D. Modulation Method

Many modulation methods such as PSPWM, triangular PWM, and trapezoidal PWM are proposed for isolated-stage DC-DC converters, of which PSPWM is the most widely used one [12]. Among many modulation techniques for MMCs proposed by many researchers, multi-carrier pulse width modulation methods such as level-shifted PWM(LSPWM) and phase-shifted pulse width modulation (PSPWM) are frequently employed for MMC-based modular converters made of low-voltage modules.

In level shift, the PWM distribution of the switching signal is uneven and hence creates uneven switching losses and unbalance of sub-module capacitor voltage. It needs a capacitor balancing algorithm which adds complexity to the modulation circuit as the number of voltage levels increases.

In the case of PS-PWM, the SM capacitor voltage is balanced with a PI controller, and the need to use a sorting algorithm can be avoided. Moreover, the switching signals are evenly distributed in the entire sub-modules, resulting in an equal distribution of switching losses in the converter. The advantage of PS-PWM over LS-PWM is highly observed if the required output voltage level number is large [12]-[14].

To generate the switching signals for a multilevel converter having “N” sub-modules per leg arm, the “N” number of carrier signals is required. The phase difference between consecutive carriers can be found using the equation below:

$$\theta = 360/N \quad (18)$$

However, to produce an output voltage having $2N+1$, the signals between upper arm and lower arm sub-modules have a phase difference given by

$$\theta = \frac{180}{N} \quad (19)$$

Phase-shifted PWM signals are generated by comparing the reference voltage (modulating signal) with a triangular waveform (carrier signal) within a comparator block. This comparison determines the converter's switching sequence: the comparator outputs a high signal (1 = switch ON) when the triangular wave exceeds



the reference voltage, and a low signal (0 = switch OFF) when it is lower. The switches in each leg of the HBSM and FBSM operate in a complementary manner to prevent short circuits. To avoid switching overlap between the upper switch and lower switch in the sub-module, a small dead time (delay time) is added to the PWM signal after the comparator block. The PS-PWM signal generation technique inside the comparator block for two sub-modules ($N=2$) is demonstrated by the signal diagram in Fig. 6 [14].

Using an MMC-based back-end converter allows the number of output voltage levels to be doubled within the same structure. This is achieved by applying interleaved phase-shift modulation with a π phase angle between the upper and lower arm carriers. This feature of MMC-based BEC gives output voltage with better THD values [15].

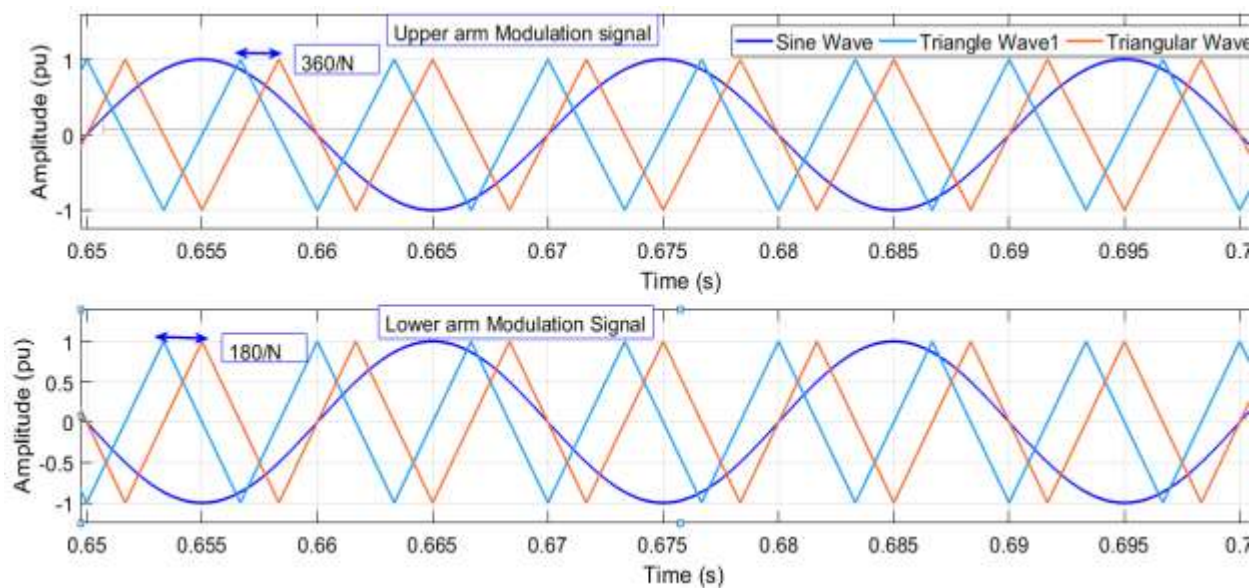


Fig. 6.: Interleaved Phase Shift Modulation

To leverage this advantage, the interleaved phase modulation technique is employed in this project.

E. Solar PV Array Sizing

Solar PV as a renewable energy source is drawing much attention in the day-to-day life of the global power industry. This is because of its free, clean, abundant, green nature, and low running cost characteristics. The maximum irradiance at a 15-degree tilt angle in Arba Minch is 2006 W/m^2 . However, the average global irradiance per day varies between 500 to 1000 W/m^2 .

The PV system faces two main challenges. First, its power generation efficiency is low. Second, the amount of electricity produced by solar panels keeps changing due to variations in sunlight caused by clouds, birds, trees, and other obstacles. The current-voltage (I-V) characteristic of a PV array is nonlinear and changes

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



with both sunlight intensity and temperature. When sunlight changes, it mainly affects the current generated by photons, with little impact on the open-circuit voltage. In contrast, temperature changes have a greater effect on the open-circuit voltage, while the short-circuit current changes only slightly. There is a specific point on the I-V or V-P curve called the maximum power point (MPP), where the PV system, including the array and converter, operate at its highest efficiency and delivers maximum output power. The exact position of the MPP is not constant but can be found using calculation models or search algorithms. However, by using maximum power point tracking (MPPT) algorithms [16], the PV system's efficiency and reliability can be greatly improved, as these algorithms continuously adjust the operating point of the PV panel to stay at the MPP according to changing irradiation and temperature conditions. An incremental conductance algorithm is used in the back-boost converter to handle the problem of MPPT. This algorithm compares the incremental conductance with the instantaneous conductance in the PV system. Based on the comparison, it adjusts the voltage, either increasing or decreasing it, until the maximum power point (MPP) is reached. Fig. 7 shows the power-voltage characteristics of the Sunpower-SPR-415E-WHT-D PV module at 25°C under different irradiance levels.

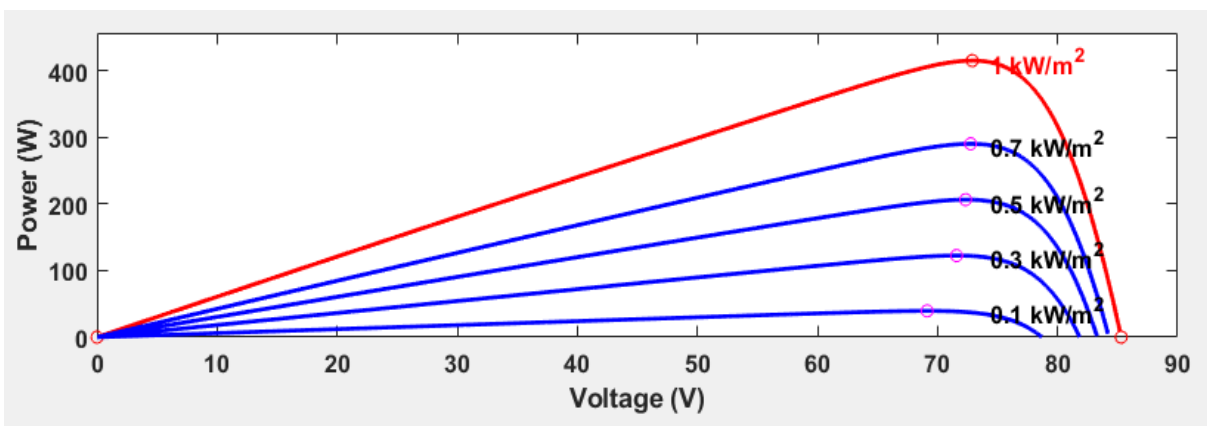


Fig. 7.: P-V Characteristic Curve of Solar PV Module at Different Irradiance

In this research, a solar PV module (Sunpower-SPR-415E-WHT-D) is used. The module has an open circuit voltage of 85.3V; voltage at maximum power is 73V and it has a maximum power of 414W. The designed system should supply a maximum power demand of 50kW, at 230V (PN). For an MMC-based modular inverter made of four modules, the input DC voltage should be 700V obtained from the output of the boost converter connected to the solar panel to get the 230V (PN) AC. The total number of solar PV modules required to supply the load is the ratio of load power demand to solar module maximum power.

$$\text{No solar modules} = \frac{\text{Load demand}}{\text{Maximum power of Solar PV module} \times \eta} \quad (20)$$

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



If the efficiency of the PV array and that of the buck-boost converter is considered to be 85%, the total number of modules required is 166.

The series connected modules and parallel strings are decided by the total output voltage obtained at the solar PV array i.e., 240V.

$$\text{No of series-connected modules} = \frac{\text{Array output Voltage}}{\text{Module voltage at Maximum power}} \quad (21)$$

The total DC voltage requirement at the LV DC link is 240V and substitution of this value in the above equation gives the number of series connected modules to be $3.28 \approx 4$, which gives the number of parallel module strings to be 42.

F. Battery Sizing

The battery acts as an external energy storage unit that absorbs or supplies power depending on the instantaneous load condition. The charging and discharging rates are determined according to the standard specifications provided in the battery handbook. Lead-acid batteries are preferred for standalone applications because they are low-cost and easy to maintain. According to the handbook of the lead acid battery, the charging current of the battery should be less than $0.1CB$, where “ CB ” is the capacity of the battery in ampere-hour (Ah). For a 200 Ah battery the charging current should not exceed 20 A [Battery Charging Current = $0.1 \times 200 = 20\text{A}$]. Also, according to the battery handbook, the discharge current in tens of seconds should not exceed $(0.5-0.7) CB$ and the nominal discharge is $0.1CB$. Here $(CB/5)$ is selected as the maximum discharge current. The sizing of the battery is similar to sizing the solar PV as done before in section 3.5. For a given load power to be delivered by the battery through a boost converter, the maximum capacity can be obtained as given below [17]: -

$$C_B = \frac{P_o}{0.1 * \eta_{Conv} * V_{Bat}} \quad (22)$$

For a system load power of 50kW, buck-boost converter efficiency of 95%, and battery voltage of 24V, the total capacity of the battery is equal to **21930Ah**. If the selected single lead acid battery has a capacity of **200Ah**, a total of **110** batteries are used to supply the system.

G. Buck-Boost Converter

The output voltage from solar photovoltaic (PV) panels is quite low, so it cannot be directly connected to a high-voltage load or the grid. To make this connection possible, a non-isolated DC-DC converter with high voltage gain is needed to interface with the solar PV system. The boost converter is placed between the modular inverter and the solar PV so that the output voltage remains fairly constant with variations in solar irradiance. In the absence of solar power, the system gets power from the battery storage system. During



normal operation (sufficient solar energy) the battery is charged through the buck-boost converter and stores energy. During night times and cloudy times, the stored battery power supplies the load through the boost converter. Depending on the charging and discharging condition of the battery sensed, the duty cycle of the buck-boost converter is changed. When the battery is in charging mode, the buck-boost converter operates in buck mode and when the battery is discharged, it operates in boost mode. The Duty cycle in charging mode is 0.12 and 0.90 when the battery is in discharging mode.

IV. Simulation Result and Discussion

A. Simulation of Isolated DC-DC stage

The input to this converter is an HVDC transmission network or grid-connected modular rectifier. If the input is obtained from a rectifier connected to the grid having a line voltage of 15kV, a maximum DC voltage of 24.5kV can be obtained, which feeds the isolated DC-DC stage and is depicted in Table III. Primary and Secondary DAB Voltage is depicted in Fig. 8.

Table III: Basic Specification of Isolated DC-DC Converter

Name of Converter	Parameter	Value
Isolated DC-DC Converter	V _{in} (nominal)	24.5kV DC
	V _{out}	240V DC
	P _{MAX}	50kW
	Switching frequency	20kHz
	C _o	10mF
	Turns ratio	36:1

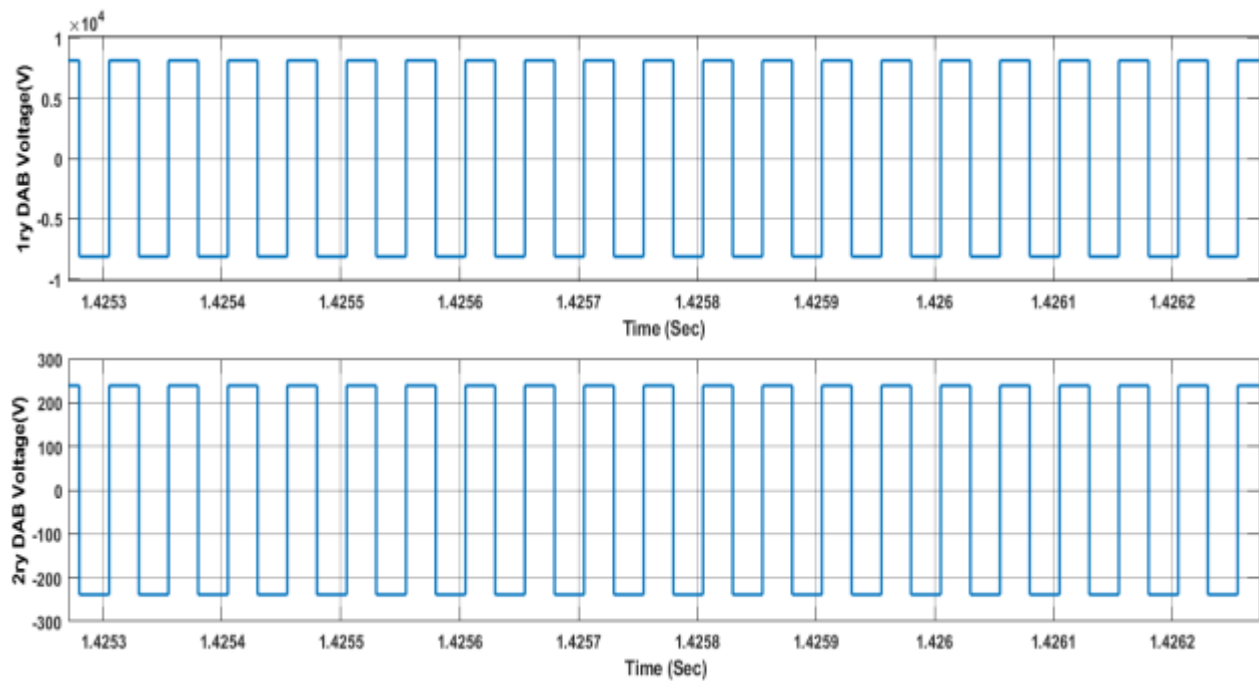


Fig. 8.: Primary and Secondary DAB Voltage

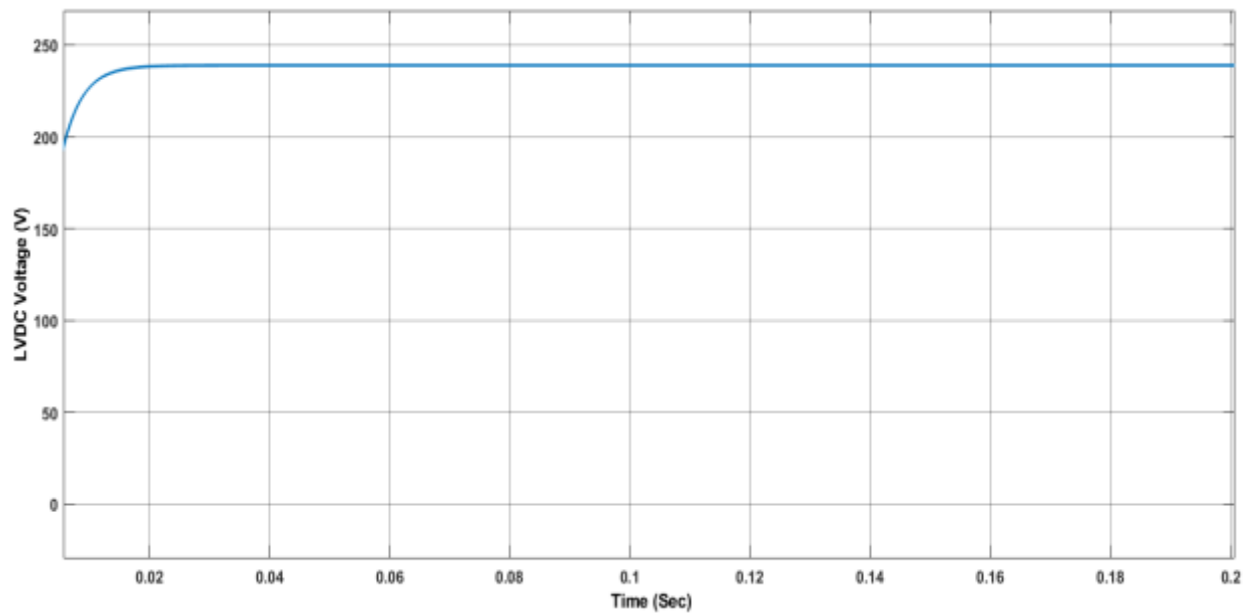


Fig. 9.: LVDC Voltage

Observation: As shown in Fig. 9 and Fig. 10, the primary DAB converters share a total input voltage of 24.5kV. Each DAB converter has a value equal to 8kV. Also, the secondary DAB has a peak voltage of 240V.

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**

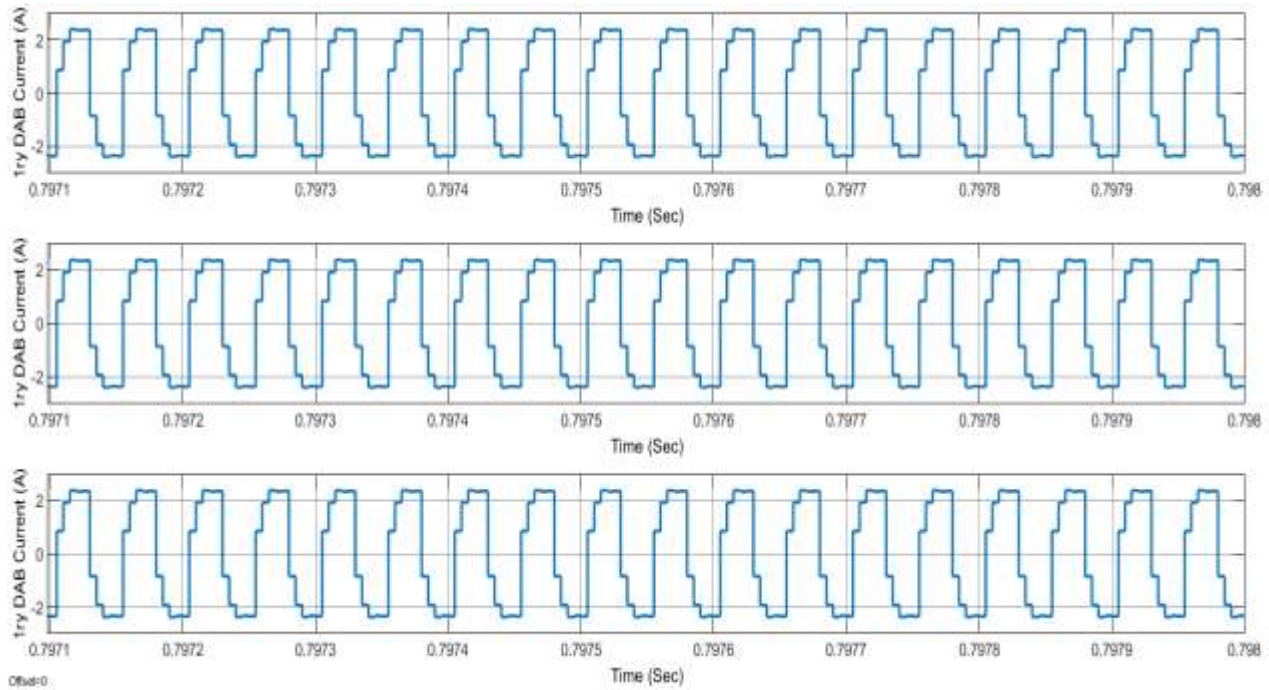


Fig. 10.: Primary DAB Currents

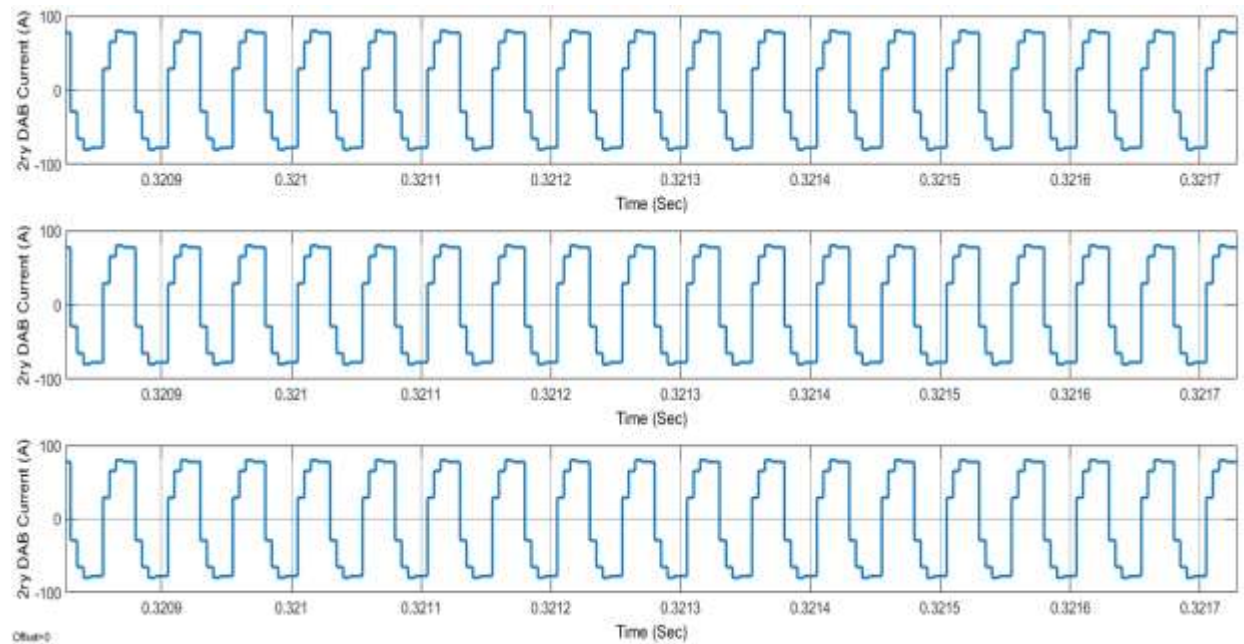


Fig. 11.: Secondary DAB Current

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**

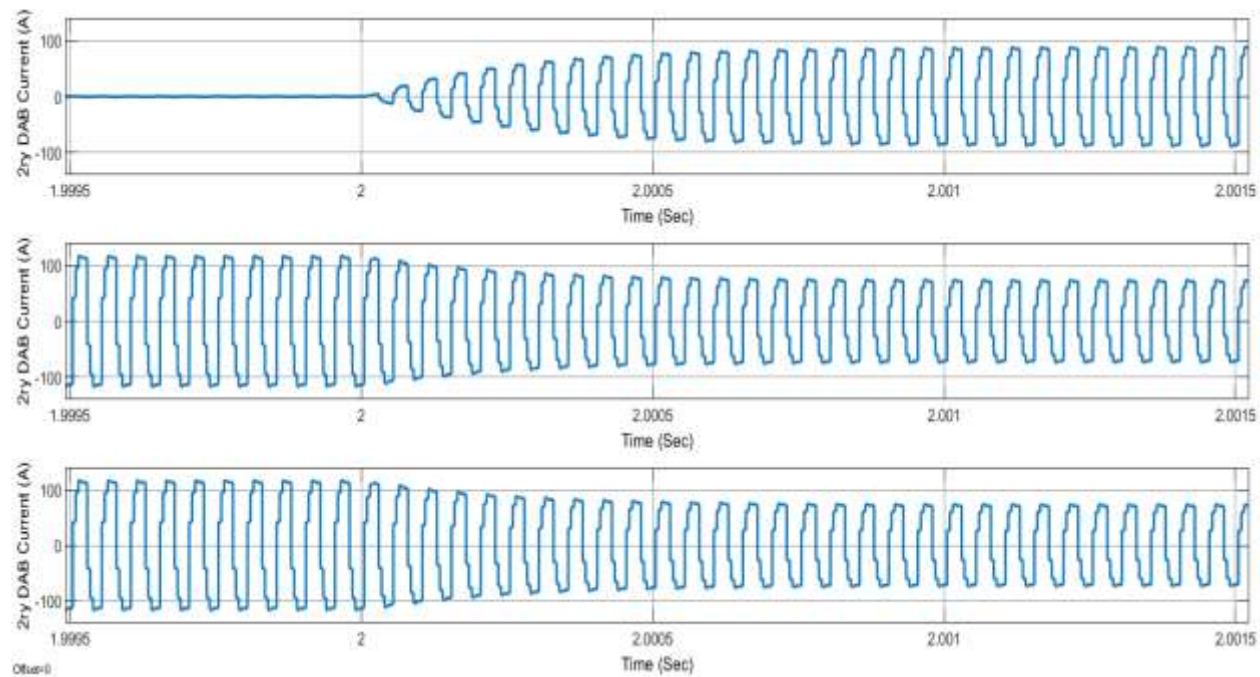


Fig. 12.: Secondary DAB Currents during Fault at DAB_1

Observation: As shown in Fig. 11 and 12, the three primary and secondary DABs share the load current equally when all are active. But, when there is a fault in any one of the DABs (secondary DAB in this case), the load current is shared among the un-faulted DABs as shown in Fig.12. This fault-tolerant feature of the system is very important in increasing the reliability of the overall system and reducing switching loss during light load conditions.

B. Simulation of Modular Inverter Fed with Solar PV

For simulating the models of modular inverters based on MMC topologies, three three-phase star-connected inductive loads (R-L load) having a maximum demand of 50kVA and a power factor of one (1) are used. Also, a maximum solar irradiance of 800W/m² and a cell temperature of 45⁰C is used as an input parameter for the Solar PV array. A steady-state system analysis is used to see changes in output voltage and current.

In Tables IV and V, the parameter values of the distribution system, converters, and solar PV module are listed. These absolute values were incorporated into the Simulink /PLECS modeling to create the system.



Table IV: Technical Specification of Modular Inverter

Parameters	Value
Output AC Line Voltage(V_g)	415V
Load resistance (R_L)	3.27 Ω
Load inductance (L_L)	5.5 μ H
Maximum Power(S)	50kW
Load Power Factor	0.95 to 1 lagging
Sub-module arm inductance (L_{arm})	3mH
Sub-module arm resistance (R_{arm})	0.1 Ω
Sub-module arm capacitance (C_{SM})	20mF
Capacitance at DC link ($C_{DC\ Link}$)	10mF
Distribution system frequency(f_g)	50Hz
Carrier frequency (f_c)	1000Hz
Modulation index	1
Boost converter duty cycle (D)	0.68
Input DC Voltage to the inverter	240V
No of Sub-module per arm (SM)	4

Table V: Technical Specification of Solar PV Array and Its Accessories

Name of Component	Parameter	Value
Solar PV(Sunpower-SPR-415E-WHT-D)	V(open circuit)	85.3V
	V(@Maximum power)	73V
	$P_{Max}/Module$	414.8W
	Maximum Irradiation	800kW/cm ²
	Cell temperature	45°C
Battery	Capacity(C_B)	200Ah
	I_{DCH}	0.1 C_B
	V(open circuit)	26V
Buck-Boost Converter	Duty cycle	0.11/0.90

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



Switching Frequency	5kHz
V_{in}/V_{out}	240V/24V(buck mode)
V_{in}/V_{out}	24V/240V(Boost mode)

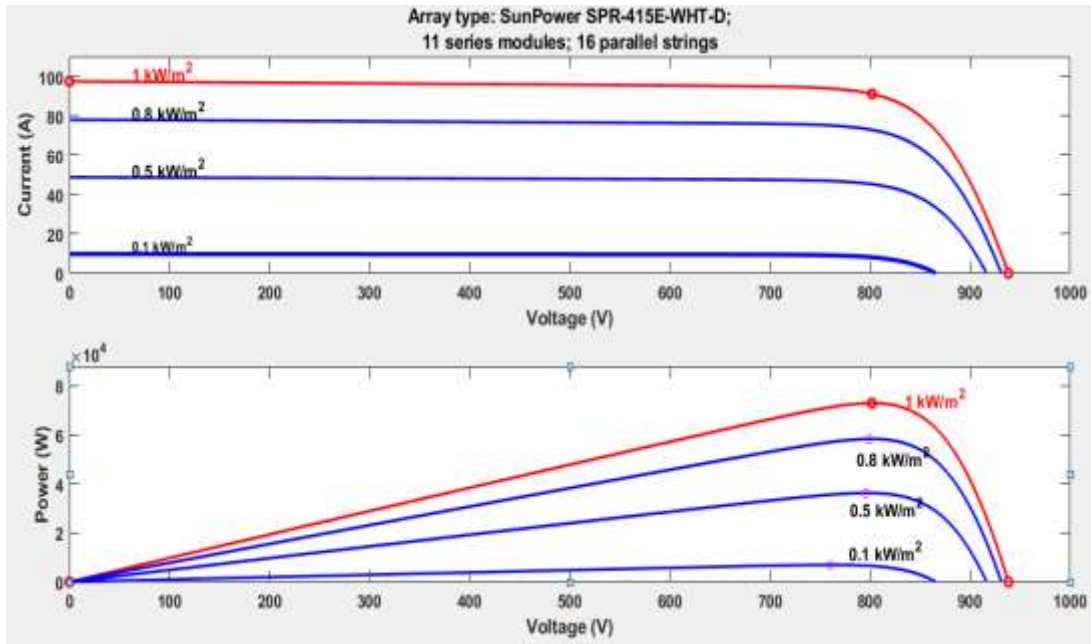


Fig. 13.: Power Versus Voltage and Current Versus Voltage Curve of PV Array

Observation: The PV array supplies the required maximum power demand of 50kW when the solar irradiance is 800w/m²

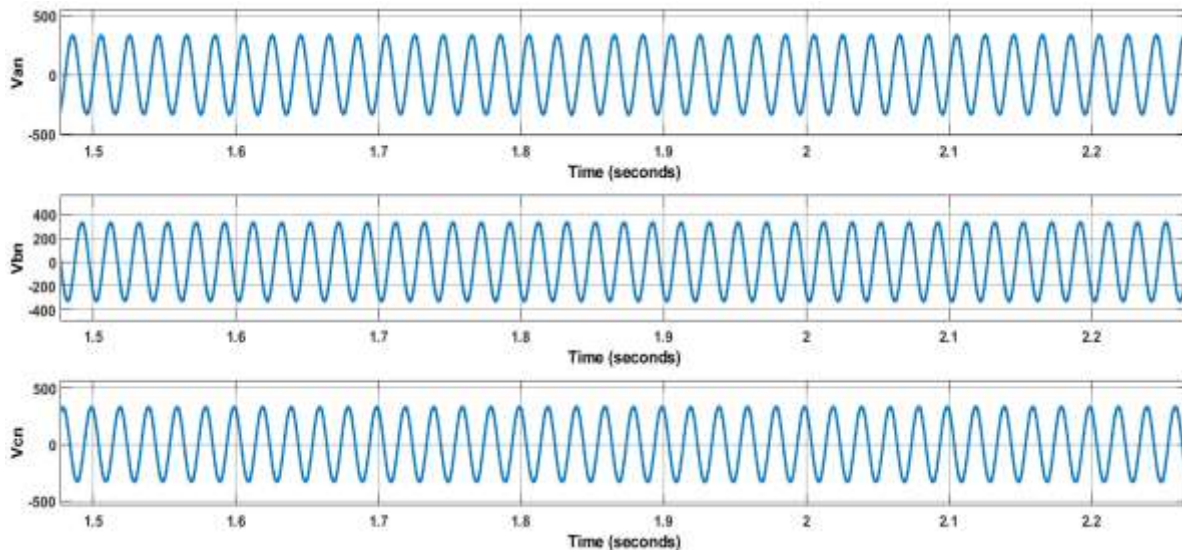


Fig 14. Voltage Wave Shape at Modular Inverter Output

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**

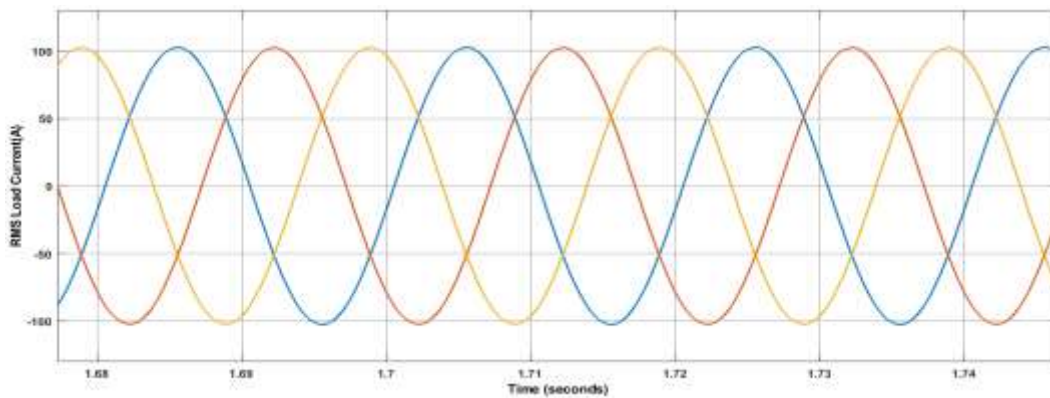


Fig. 15.: Three Phase Load Current Wave Shape of Modular Inverter

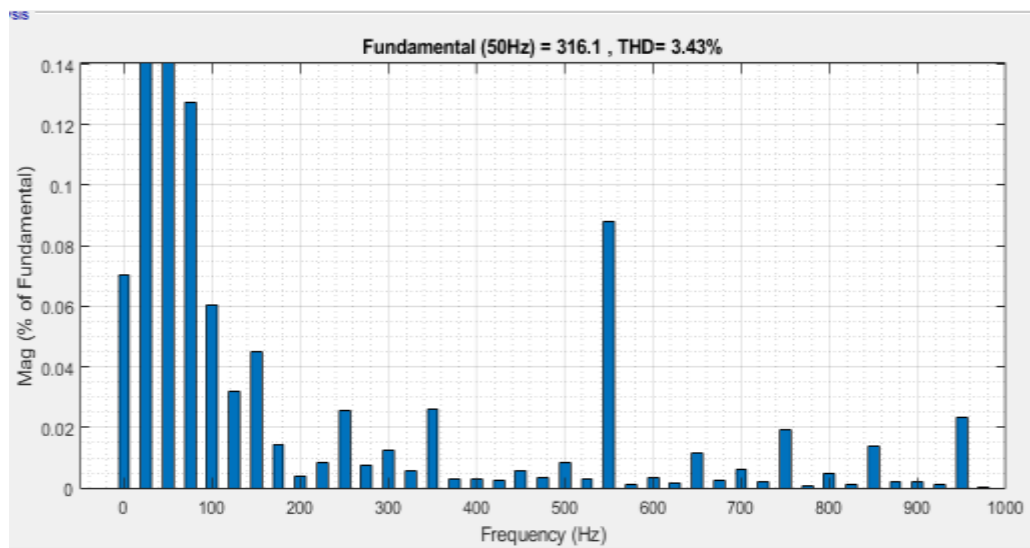


Fig. 16: Voltage THD at Modular Inverter

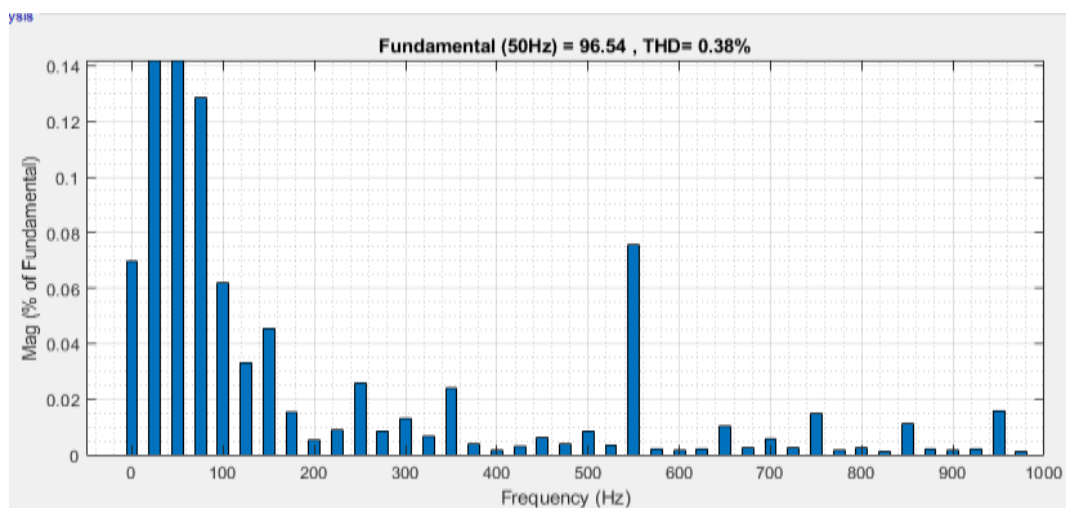


Fig. 17: Current THD at Modular Inverter Output

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



Observation: As shown in Fig. 14 to Fig. 17, the modular inverter output voltage is 230V (PN) when delivering a load current of 73A RMS. Also, the voltage and current THD values are 3.43% and 0.38% respectively, both within the IEEE 519-1992 benchmark. The losses happening in the converter and its achieved efficiency are presented in Table VI and Fig. 18 below: -

Table VI: Semiconductor Losses

Device Name	Switching Loss(W)	Conduction Loss (W)	Total Loss (W)	Efficiency (%)
MOSFET	1029.54	818.69	1848.23	96.63

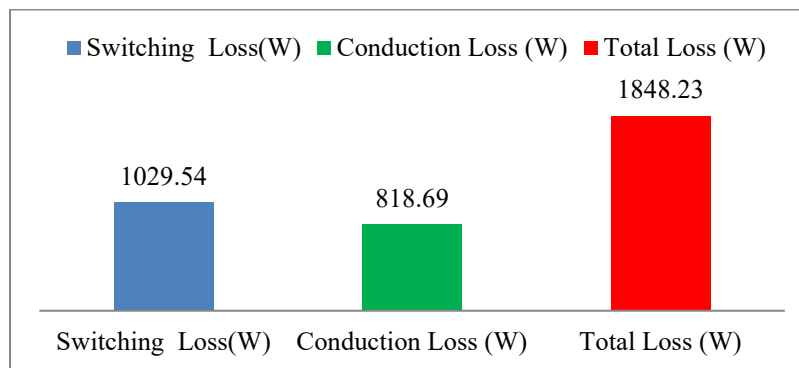


Fig. 18.: Switching and Conduction Losses

Based on the result in Fig. 18 and equation (27), the efficiency of the system is calculated to be 96.63%.

V. Conclusion

In this research design modeling and technical evaluation of multiport converter-based hybrid power supply for a small village having a maximum demand of 50kW has been done. The multiport converter system contains an isolated DC-DC converter and modular inverter. The isolated DC-DC converter is based on DAB-ISOP configuration whereas the inverter is based on MMC. The DC-DC converter operates at a switching frequency of 20 kHz whereas the modular inverter operates at a switching frequency of 1 kHz. Both converters used a phase-shifted PWM to generate a gating signal. Solar PV array having an output voltage of 240V is used as input to the modular inverter. Also, the system is integrated with battery storage to increase the reliability of the whole system. The battery is charged and discharged through a buck-boost converter having a duty cycle of 0.11(buck mode) and 0.90(boost mode). Simulation results showed that the proposed system is a viable alternative to a low-frequency transformer with many ancillary services such as RES integration and improved availability.

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



References

1. M. A. Hannan, P.J. Ker, M. S. Hossain L., Z. H. Choi¹, M. S. Abd. Rahman, K. M. Muttaqi, and F. Blaabjerg, "State of the art of solid-state transformers: Advanced topologies, implementation issues, recent progress and improvements", *IEEE Access*, vol. 8, pp 19113-19132, Jan. 17, 2020.
2. L. Wei, L. Gregoire, J. Bélanger, "Control and performance of a modular multilevel converter system," *CIGRÉ Canada Conf. on Power Systems*, Halifax, Sept. 2011, pp. 1-8.
3. A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *Power Tech Conf. Proceedings, 2003 IEEE Bologna*, Italy, 2003, vol. 3, pp. 1–6.
4. L. F. Costa, F. Hoffmann, G. Buticchi, and M. Liserre, "Comparative analysis of mab dc-dc converters configurations in modular smart transformer," *IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, April 2017, pp. 1–8. DOI10.1109/PEDG.2017.7972558
5. M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
6. L. Wei, L. Gregoire, J. Bélanger, "Control and performance of a modular multilevel converter system," *CIGRÉ Canada Conf. on Power Systems*, Halifax, pp. 1-8, Sept. 6-8, 2011.
7. Y. Zhang, G. P. Adam, T. C. Lim, S.J. Finney, B.W. Williams, "Analysis of modular multilevel converter capacitor voltage balancing based on phase voltage redundant states", *IET Power Electron.*, vol. 5, no. 6, pp. 726–738, July 2012.
8. Ali Shojaei, "Design of modular multilevel converter-based solid state transformers", M.S. Thesis, Dept. of Elect. and Compt. Eng., McGill Univ., Montreal, Canada, November 2014.
9. J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," *15th International Power Electronics and Motion Control Conf. (EPE/PEMC)*, 2012, pp. LS1a-1.1-1-LS1a-1.1-8.
10. <http://www.plexim.com> (PLECS User Manual), Jan 14, 2022.
11. <http://www.irt.com/pachage/> (IRFP4668PbF datasheet), Jan 14, 2022.
12. S. Debdnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review", *IEEE Transactions On Power Electronics*, vol. 30, no. 1, pp. 37-53, Jan. 2015.
13. S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses and semiconductor requirements of modular multilevel converters", In *IEEE Transactions on Industrial Electronics*, vol.

Received: May 30, 2023; **Revised:** 08 October 2023; **Accepted:** 09 October 2023; **Published:** 31 December 2023.

Corresponding author- **Yalisho Girma**



-
- 57, no. 8, pp. 2633–2642, 2010.
14. Yalisho Girma, Getachew Biru, Chandra Sekhar “A comparative study on modeling and performances of modular converter based three-phase inverters for smart transformer application”, *Journal of Science and Inclusive Development*, vol. 5, no. 2, pp. 91-115, 2023. <https://doi.org/10.20372/jsid/2023-256>.
 15. T. Kaliannan, J. R. Albert, D. M. Begam and P. Madhumathi, “Power quality improvement in modular multilevel inverter using different multicarrier PWM” *European Journal of Electrical Engineering and Computer Sciences*, vol. 5, no.2, 2023. <http://dx.doi.org/10.24018/ejece.2021.5.2.315>
 16. M. Park and I-K. Yu, “A novel real-time simulation technique of photovoltaic generation systems using RTDS,” *IEEE Transactions on Energy Conversion*, vol. 19, no. 1, pp. 164–169, 2004.
 17. S. Saravanan, S. Thangavel, “A simple power management scheme with enhanced stability for a solar PV/wind/fuel cell/grid fed hybrid power supply designed for industrial loads”, *Journal of Electrical and Computer Engineering*, vol 2014, Art. ID 319017, 2014. <http://dx.doi.org/10.1155/2014/319017>